REMARKS

Claims 1-9 stand rejected under 35 U.S.C. 102(b) as being anticipated by Reeve et al. (U.S. 5,535,393). Applicants respectfully traverse this rejection because the cited reference does not disclose (or suggest) private interface areas that are dynamically allocated for non-master threads, as in claims 1-8 of the present invention, nor does the reference disclose access to an interface area based on whether an active thread is a master thread and common block information for the interface area is new, as in claim 9 of the present invention.

The Examiner has not established a *prima facie* case of anticipation against any of the claims of the present invention. None of the text portions cited by the Examiner from Reeve support the Examiner's assertions as to what these text portions teach. Reeve teaches a parallel processing system that focuses primarily on tile management. Reeve further describes the use of threads, including master threads (col. 30, lines 53-54 for example), and interfaces (col. 17, line 35 to col. 19, line 31; col. 31, line 33 to col. 37, line 56). Nowhere, however, does Reeve teach or suggest the private interface areas of the present invention or, more particularly, that private interface areas are dynamically allocated for non-master threads.

With respect to independent claim 1 and 5 of the present invention, none of Reeve's description from the Summary of the Invention, col. 7, or col. 54 are analogous to the features of the present invention as asserted by the Examiner on page 2 of the outstanding

Office Action. Reeve's Summary of the Invention focuses on tile management for the parallel processing system, and gives no direction to one skilled in the art for allocation of interface areas for master threads or non-master threads. The text from col. 7 is similarly lacking, because it only generally describes directives for parallel processing, but remains silent regarding interface areas for threads. The text from col. 54, on the other hand, is actually only a claim, and one that deals with allocating space for tiles, but does not recite threads or interface areas.

This rejection is therefore particularly deficient because Reeve expressly distinguishes between tiles, tile allocation, threads, and interface areas, with no ambiguity between the different meanings of these terms. Reeve further defines subroutines and procedures, and affinity regions (col. 27, line 26 to col. 28, line 11; col. 39, line 61 to col. 42, line 7), and all as different elements than threads or tiles. All of these terms are clearly defined by Reeve, and there is no confusion between their meanings. Accordingly, because Reeve clearly defines the use of threads and interface areas in the cited reference, and because none of the text portions cited by the Examiner from this reference with respect to claims 1 and 5 teach or suggest anything regarding these features of the present invention, the rejection of these claims is respectfully traversed and should be withdrawn.

With respect to independent claim 9 of the present invention, the cited portions are equally deficient regarding any teaching or suggestion of utilizing an object code to dynamically allow access to an interface area according to whether an active thread is a

master thread, or whether common block information for the interface area is new. As discussed above, the portions of text from Reeve cited by the Examiner against claim 9 remain silent regarding interface areas, master threads and new common block information for an interface area. Accordingly, the Examiner should be required to state exactly what elements from Reeve he finds analogous to the present invention, or withdraw the rejection in its entirety.

With respect to independent claims 2 and 6 of the present invention, the rejection is also deficient for reasons similar to those above. Against claims 2 and 6, the Examiner cites text portions only from cols. 35 and 43 of Reeve. Neither text portion, however, describes anything relating to interface areas, or the allocation of private interface areas for non-master threads. The text from col. 35 does describe master and non-master threads, but only with respect to the allocation of *affinity regions*. As discussed above though, affinity regions are different than interface areas. The text from col. 43 describes "interface *environment variables*" with respect to master and non-master threads, but does not teach or suggest anything regarding the allocation of private interface areas for non-master threads, as clearly recited in both claims 2 and 6 of the present invention.

The cited text from col. 35 further fails to support the Examiner's assertion that it teaches an object code that determines the leading addresses of private interface areas which are dynamically allocated for non-master threads instead of the common interface area, when one of the plurality of threads is processed. This portion of the Reeve reference merely

discloses a single subroutine called by the use of a pointer, and nothing like the relevant limitations of the claims 2 and 6 of the present invention. Claims 2 and 6 both feature the use of private interface areas that are dynamically allocated for each parallel processed thread. The leading addresses of these private interface areas are determined, and the areas are used by elements, which may even be variables, that are entirely different from the affinity regions taught by Reeve. The Examiner has not provided any rationale for how the unrelated subroutine from Reeve teaches these particular features of the present invention. Accordingly, for at least these reasons as well, the rejection of independent claims 2 and 6 is also respectfully traversed, and should be withdrawn.

With respect to claim 3 of the present invention, this claim depends from independent claim 2, and should therefore be in condition for allowance for at least the reasons discussed above with respect to claim 2. The rejection of claim 3 is further deficient because this portion of text cited from col. 42 of Reeve is irrelevant to the allocation on interface areas. Reeve describes in this text portion only the use of threads to implement critical sections and barriers, but remains silent regarding interface areas, and more particularly, the allocation of private interface areas for non-master threads.

The rejection of claims 4 and 7-8 suffers from the same deficiencies as the rejection of claim 3. First, claim 4 depends from independent claim 2 and claims 7-8 depend from independent claim 6, and therefore these dependent claims should be in condition for allowance for at least the reasons discussed above with respect to their respective base claim.

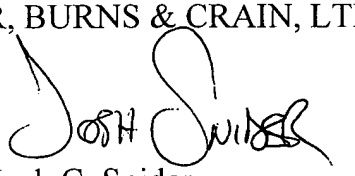
The rejection of these claims is further deficient though, because the only text portion from Reeve cited against these claims (col. 16, lines 56-64) does not teach or suggest anything regarding private interface areas for non-master threads. This portion of text only describes the implementation of an interface to thread groups, but not individual non-master. In other words, this portion of text describes only a common interface area, which is recited by the present invention as being different from the private interface areas allocated for non-master threads.

The Examiner simply has not identified one teaching or suggestion from the Reeve reference regarding the allocation of private interface areas for non-master threads. Accordingly, a *prima facie* case of anticipation cannot be established against the present invention from the Reeve reference.

For all of the foregoing reasons, Applicants submit that this Application, including claims 1-9, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

Josh C. Snider
Registration No. 47,954

Customer No. 24978

October 18, 2005

300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: (312) 360-0080
Facsimile: (312) 360-9315